TRUE CIRCUITS INC™ | *timing is everything*

Timing Challenges in the Modern SoC

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About True Circuits, Inc.

- Leading provider of high-speed analog/mixed-signal IP
- Founded in 1998, with headquarters in Los Altos, CA
- Experienced analog team, led by world-class PLL expert
- Close technical relationships with major foundries
- Customers include most semiconductor suppliers and design service providers
- Build easy to use, highly programmable hard macros in most foundries and processes variants

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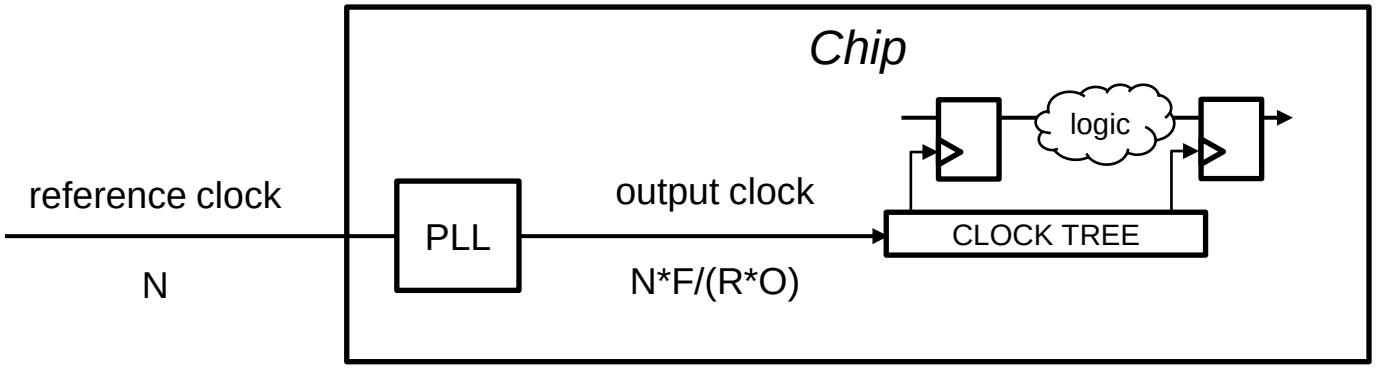
Timing Challenges

- Clock generation for synchronous logic
- Deskewing clocks
- High frequency resolution
- Spread spectrum for EMI reduction
- Using clocks to manage power
- Very low jitter
- Analog delay lines

Clock Generation

- All synchronous logic needs a clock (one per timing domain)
- High speed clocks must be created on chip (with the PLL)

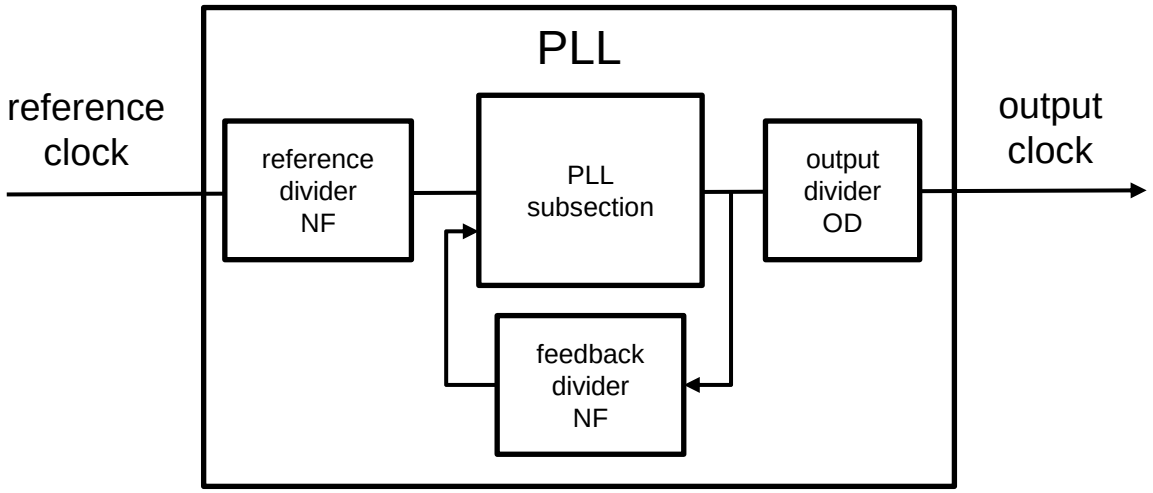


- The PLL drives the clock trees
- Closing timing: constrain clocks by worst case period jitter

max_clk * (1 + 2.5%), where period jitter is +/- 2.5%

Frequency Resolution

- Where exact frequencies are needed: RF, LCD monitors



- Output = (Ref / NR) * NF / OD
- Large dividers allow resolution and multiplication

  NF= 8192, NR=64, OD=16
- Fractional-N: more resolution

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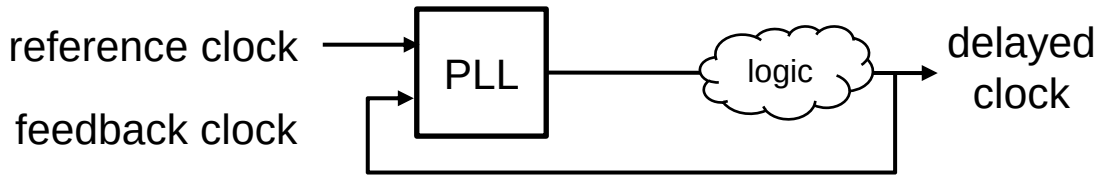
Deskew

- Deskew aligns clocks
- Aligns delayed clock to reference clock
- Can also multiply the reference clock



- Allows data to be latched between clock domains synchronously
- Could account for insertion delays

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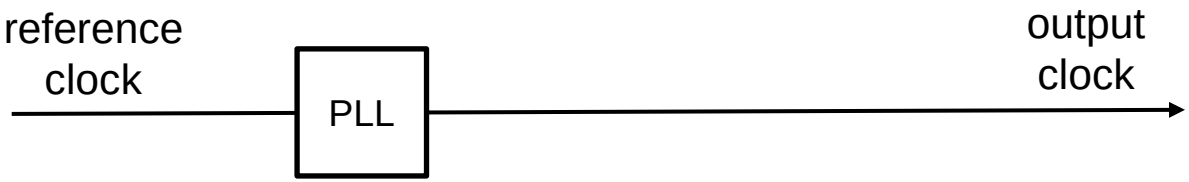
Jitter Filtering

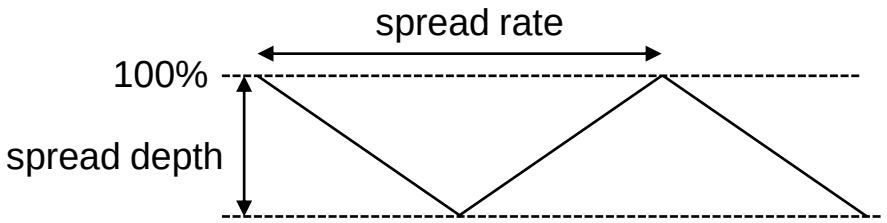
- Goal: To filter the reference clock jitter with frequencies above the PLL bandwidth



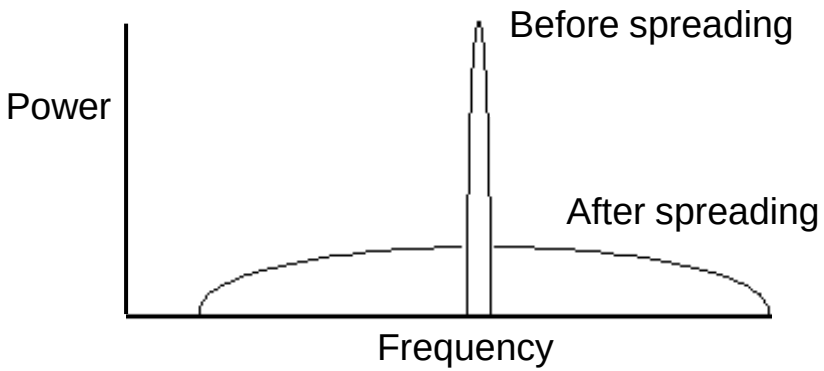
- Can adjust TCI PLL bandwidth (BWADJ)
- Care required if PLL generates reference
  - Differ PLL bandwidths to avoid jitter peaking

Spread Spectrum

- Output frequency slowly modulated



- Used to reduce emitted EMI



- Program depth: tradeoff performance vs. lower EMI

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Managing Power

- PLL reference as low as 32KHz (watch crystal)
  - IoT PLL: 8,192 multiply to 262MHz
  - Ultra PLL: 250,000+ multiply to 3.25GHz
- Can create a fine range of output frequencies to manage power
- 32KHz “heart-beat” allows very low power mode

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Low Jitter

- SerDes reference clocks need low integrated jitter
  - High frequency can cause Rx/Tx problems
  - Long-term jitter can overflow buffers
- Wireless front-ends need low jitter to reduce sampling errors
- Need low-jitter PLL, but with wide range to use generally

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TCI Ultra PLL

- State-of-the-art PLL architecture using high-speed digital and analog circuits
- Ultra low jitter (‹1ps) for the most demanding SerDes and ADC reference clocks
- Ultra wide output frequency range (10MHz to 3.25GHz) with multiplication factors over 250,000
- Precise frequency control with a least 26 fractional bits for extremely high fractional-N resolution
- Optional spread spectrum support

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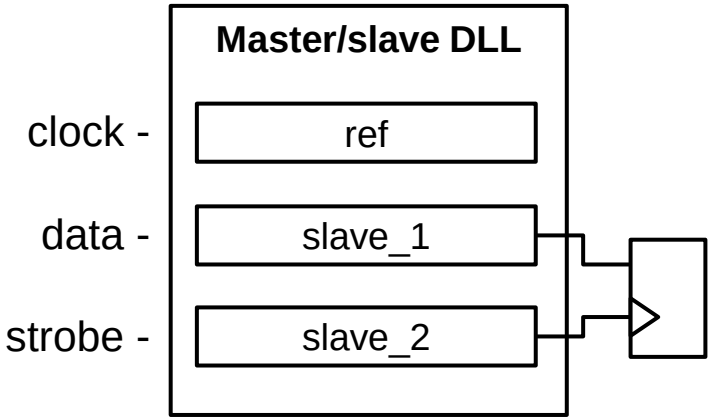
DLLs

- Master/slave PVT-compensated delay



  - Used for DDR and ONFI (NAND flash)
  - Delay and adjust strobe (DQS) to sample data (DQ)
  - Can delay for write leveling and other tuning
  - Fine resolution, with speed vs sweep tradeoff
- Multi-phase DLL: 16 evenly-spaced phases
  - Mux interpolation can be used

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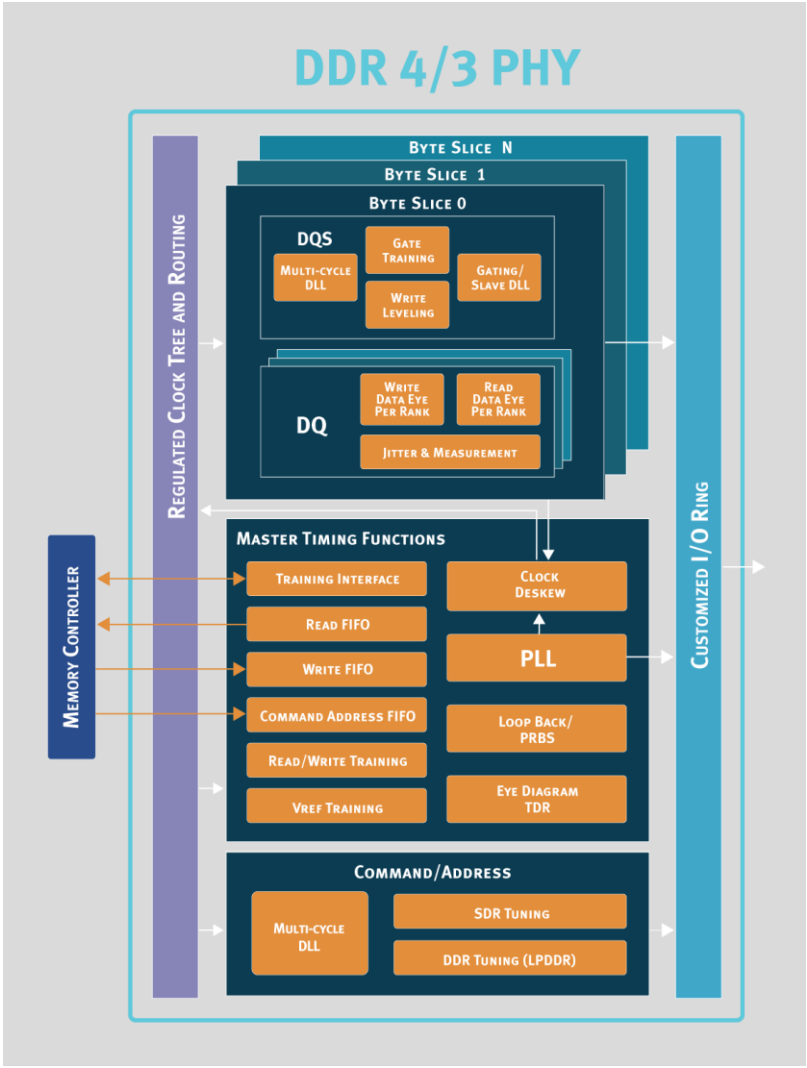
Portfolio for Timing Challenges

Product	Feature
General Purpose PLL	Deskew
	Small multiplication
Clock Generator PLL	Large multiplication
	High frequency and resolution
Spread Spectrum PLL	Fractional-N
	Spread spectrum
IoT PLL	Low power
	Run from 32KHz crystal (250MHz output)
Ultra PLL	Very low jitter
	Reference clock for high-speed interfaces
	Very high multiplication (250,000+)
DDR DLL	Master-slave DLL, perfect for DDR and ONFI
Multi Phase DLL	Creates 16 evenly spaced phases

A Timing Challenge: DDR4/3 PHY

- High-performance, scalable system
- Radically new architecture eliminates most issues with parallel interfaces (like SerDes)
- Read and gate timing are also continuously tuned by data phase, rank and pin
- All training is automatic, including multi-cycle read and write leveling, write data eye centering, and internal and external (on DRAM) Vref adjustment
- Remarkable physical flexibility to adapt to floorplan and packaging constraints
- Delivered macro: no assembly required



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Summary

- Many challenges
- Many solutions
- Need a portfolio with features and programmability

  (Available across processes, variations, metal stacks)

TCI has you covered